Rebasing Microarchitectural Research with Industry Traces

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Introduction

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- Workloads can be simulated via emulation or by extracting traces to feed a simulator.
  - Information might be lost in translation → A good workload is incorrectly simulated.

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- CVP-1 Aarch64 traces (generated at Qualcomm) are of large interest:
  - They are numerous (135 *public* and 2013 *secret*).
  - Wide range of workloads of interest: Compute INT/FP, cryptography, and datacenter.
  - They embed output register values.
  - They include system activity (typically not the case with Pin).

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- Interest in running CVP-1 traces in a microarchitectural simulator (e.g., ChampSim).

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- A CVP-1 to ChampSim converter is already available.
  - Emphasis on capturing the behavior of applications with very large instruction working sets.
    - Goal: studying instruction cache and branch predictor optimizations.
    - A subset of the traces used in the IPC-1 Championship.

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Competition traces		
Rank	Prefetcher	SpeedUp
1	EPI	1.2951
2	D-JOLT	1.2884
3	FNL+MMA	1.2861
4	BARÇA	1.2832
5	PIPS	1.2799
6	JIPS	1.2768
7	MANA	1.2658
8	TAP	1.2351

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  - No addressing mode for memory instructions.
  - No special-purpose registers.

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  - Could skew observations and lead to inaccurate conclusions.

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We revisit the CVP-1 traces and perform a thorough analysis, allowing a better conversion to the ChampSim format.

Outline

- Introduction
- Conversion of memory instructions
  - Improvement mem-regs
  - Improvement base-update
  - Improvement mem-footprint
- Conversion of branch instructions
- Experimental evaluation
- Conclusion

Conversion of memory instructions

Improvement mem-regs

CVP-1 trace format

(Relevant fields for memory instructions only and not to scale)

Conversion of memory instructions

Improvement mem-regs

```
LDP X1, X0, [X0]
```

Load pair → X1 = Mem[X0], X0 = Mem[X0+8]

Conversion of memory instructions

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Type	Address	Size	Source regs.	Dest. regs.	Written vals.
load	addr	8	X0	X1, X0	Val1, Val0

CVP-1 trace format

cvp2champsim

Memory dests.	Memory sources	Source regs.	Dest. regs.
--	addr	X0	X1

ChampSim trace format

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Memory dests.	Memory sources	Source regs.	Dest. regs.
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ChampSim trace format

Not all destination registers are conveyed in the conversion.

Conversion of memory instructions

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CVP-1 trace format

cvp2champsim

Memory dests.	Memory sources	Source regs.	Dest. regs.
--	addr	X0	X1, X0

ChampSim trace format

Convey all destination registers in the conversion.

- Dependencies with younger instructions are preserved.

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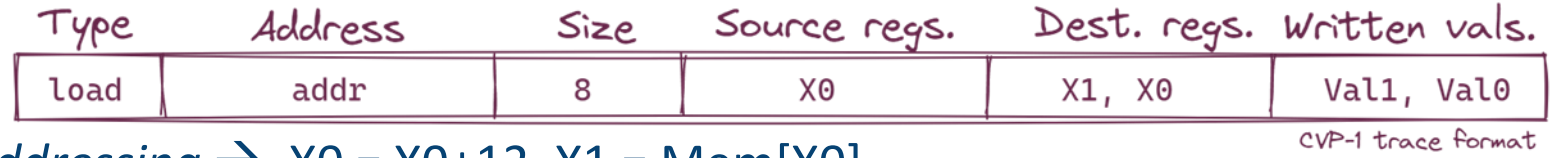
Conversion of memory instructions

Improvement base-update

```
LDR X1, [X0, #12]!
```



Load with pre-indexing increment addressing → X0 = X0+12, X1 = Mem[X0]

Conversion of memory instructions

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Conversion of memory instructions

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CVP-1 trace format

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cvp2champsim

Memory dests.	Memory sources	Source regs.	Dest. regs.
--	addr	X0	X1, X0

ChampSim trace format

No difference between:

- X0, generated by an ALU operation.
- X1, loaded from memory.

Conversion of memory instructions

Improvement base-update

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LDR X1, [X0, #12]!
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Type	Address	Size	Source regs.	Dest. regs.	Written vals.
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CVP-1 trace format

Load with pre-indexing increment addressing → X0 = X0+12, X1 = Mem[X0]

- Infer the addressing mode.
- Detect the base register.
- Differentiate between pre- and post-indexing increments:
  - Pre: ALU + MEM
  - Post: MEM + ALU

Conversion of memory instructions

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- Detect the base register.
- Differentiate between pre- and post-indexing increment:
  - Pre: ALU + MEM
  - Post: MEM + ALU

	Memory dests.	Memory sources	Source regs.	Dest. regs.
ALU:	--	--	X0	X0
MEM:	--	addr	X0	X1

ChampSim trace format

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CVP-1 trace format

Addr	Cacheline (Addr)	Addr+8	Cacheline (Addr+8)
0x0ad70030	0x0ad70000	0x0ad70038	0x0ad70000

← Belong to the same cacheline

Converted instructions access a single cacheline.

Conversion of memory instructions

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0x0ad70038	0x0ad70000	0x0ad70040	0x0ad700010

← Cross a cacheline boundary

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0x0ad70038	0x0ad70000	0x0ad70040	0x0ad700010

Cross a cacheline boundary

cvp2champsim

If an access crosses a cacheline boundary:
→ Add a second memory source.

Memory dests.	Memory sources	Source regs.	Dest. regs.
--	addr, addr+8	X0	X1, X0

ChampSim trace format

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  - Improvement flag-reg
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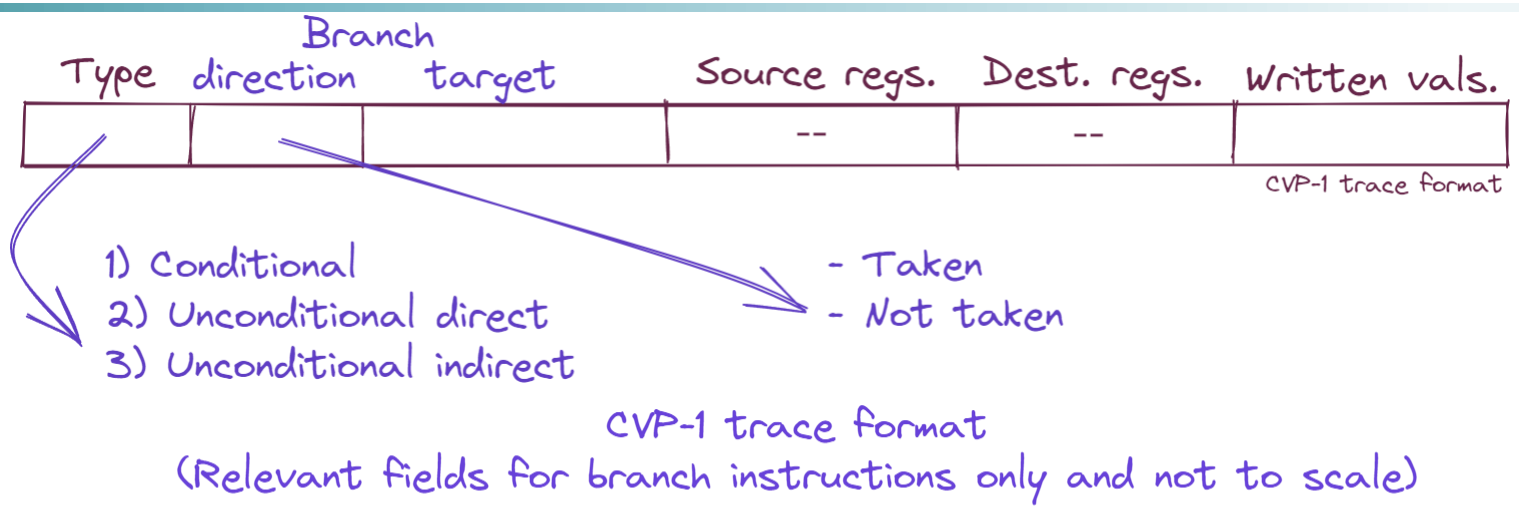
Conversion of branch instructions

Improvement call-stack



Conversion of branch instructions

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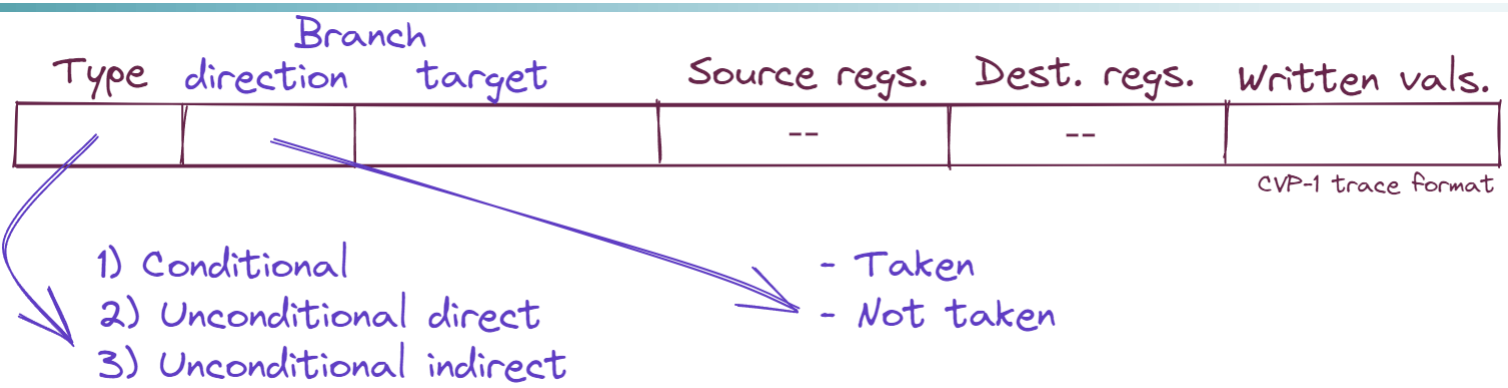

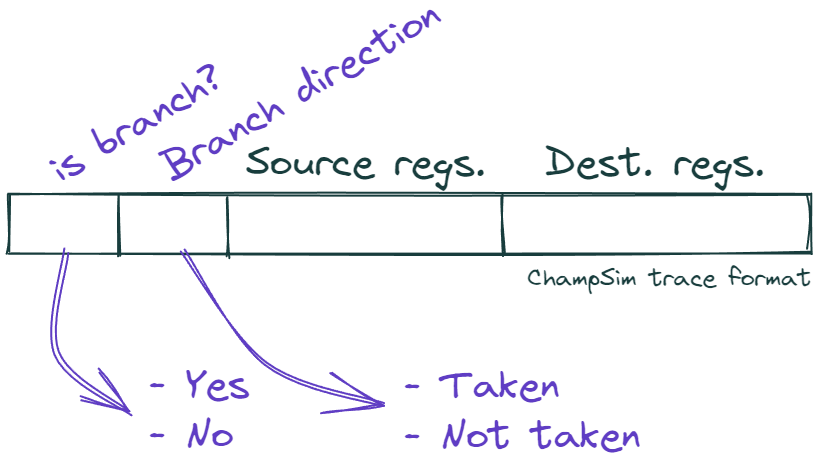

ChampSim trace format
(Relevant fields for branch instructions only and not to scale)

Conversion of branch instructions

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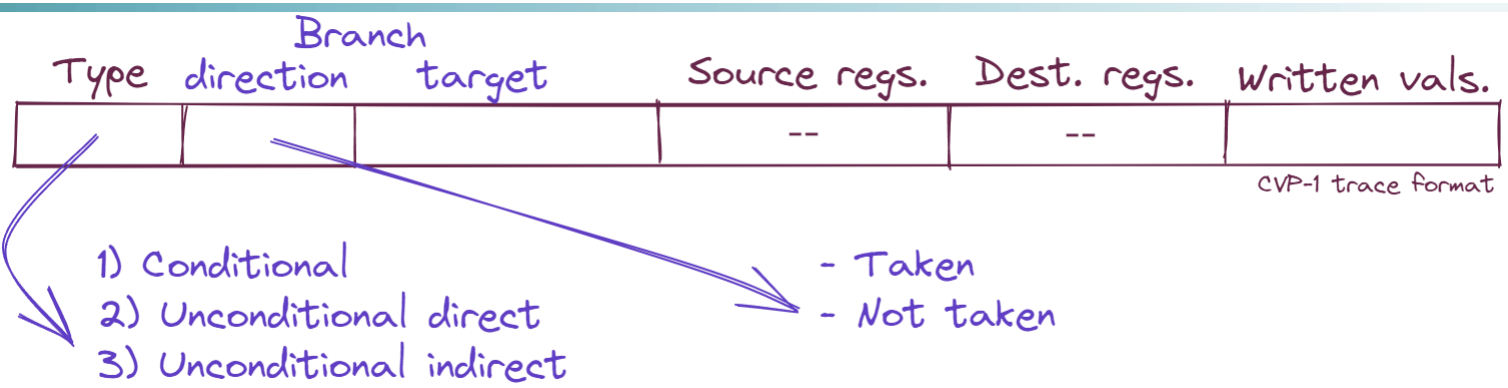
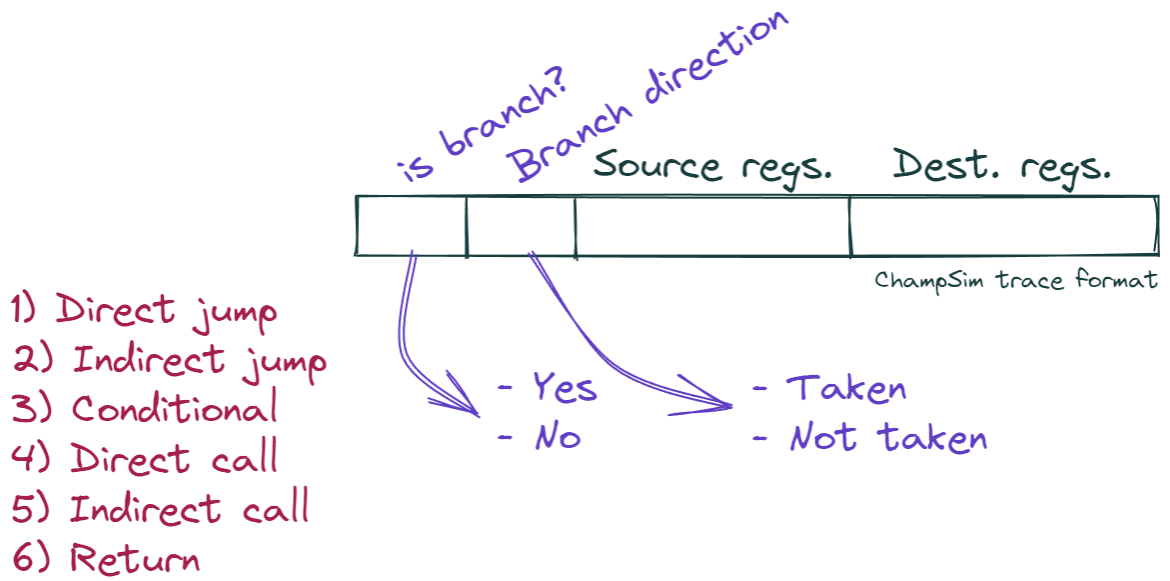
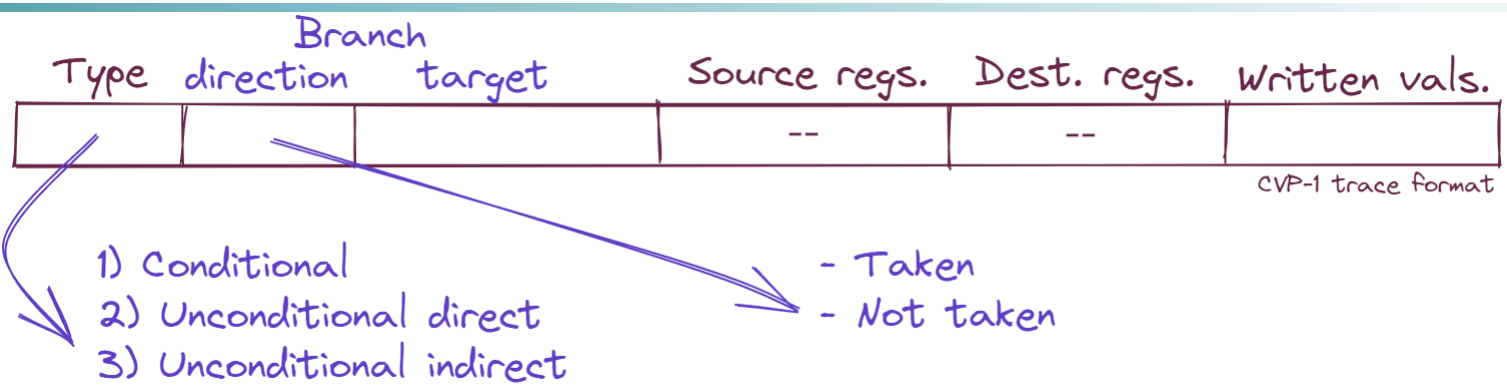
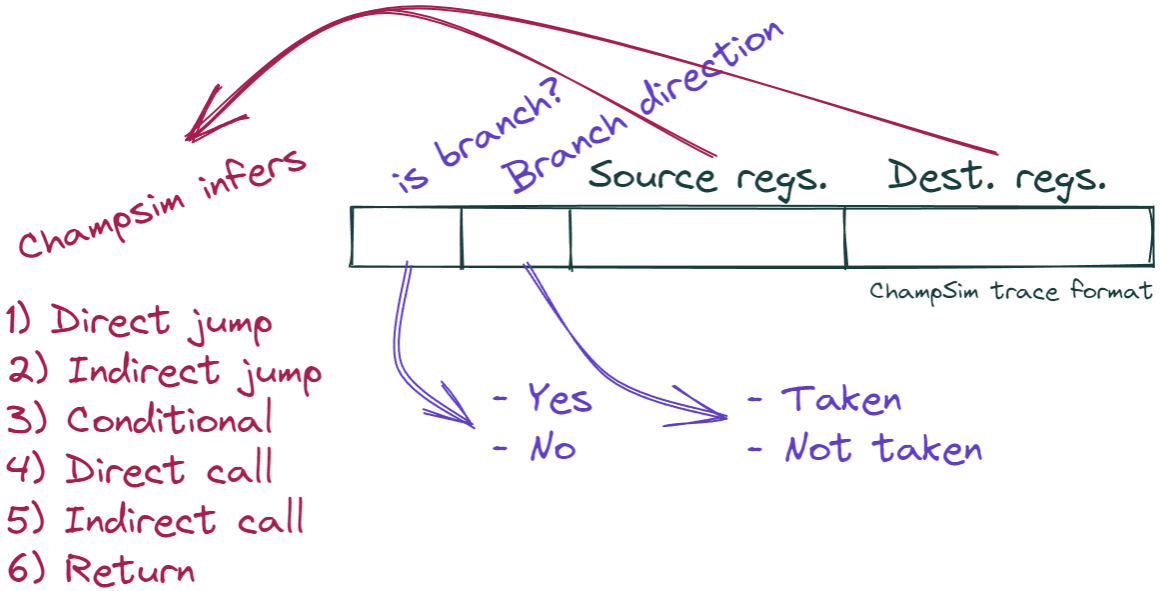




Conversion of branch instructions

Improvement call-stack





Conversion of branch instructions

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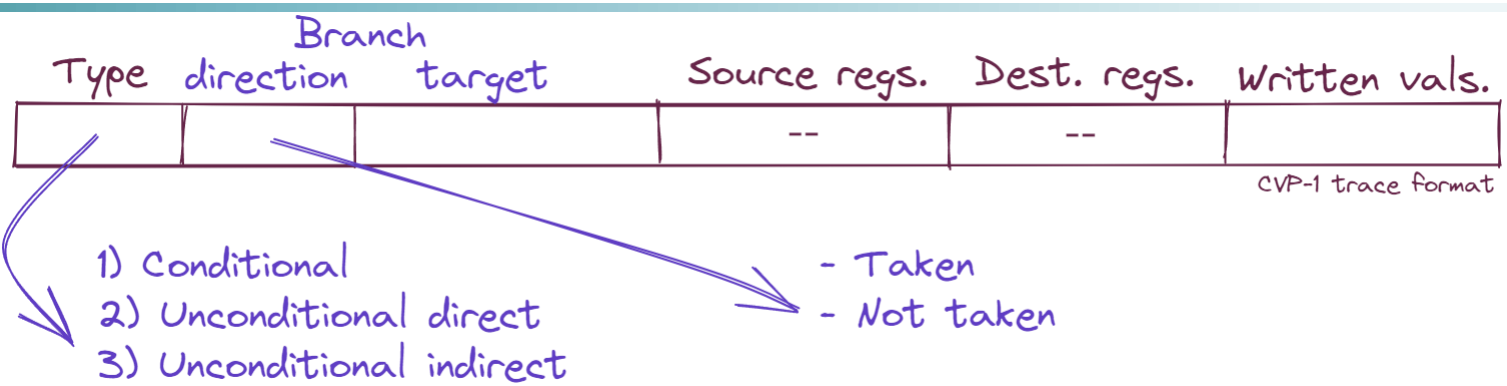
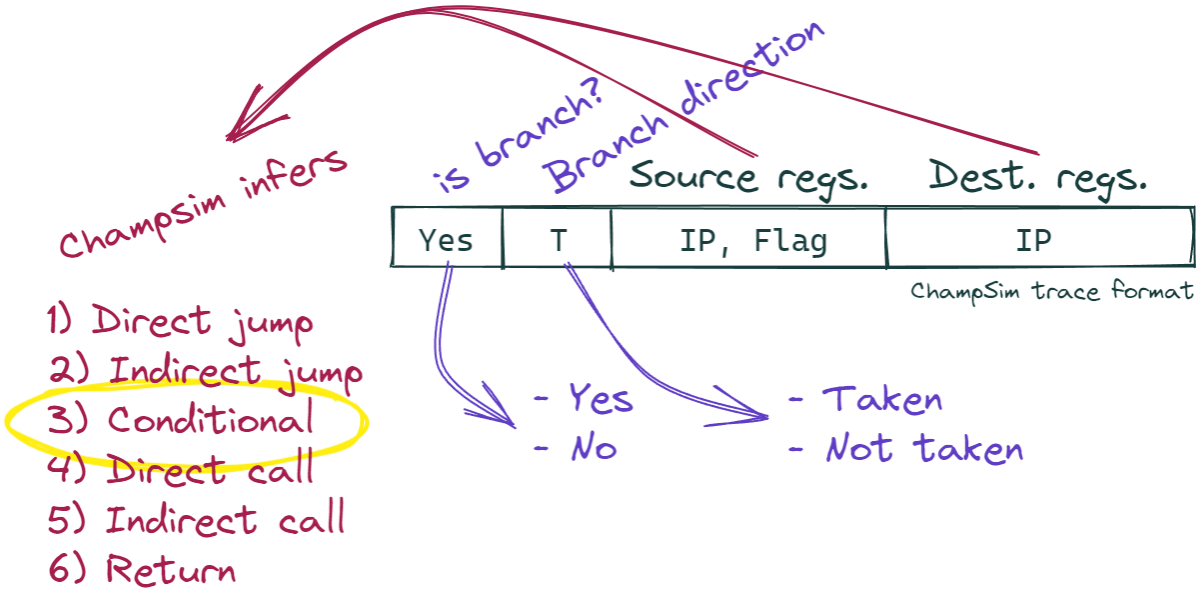




Conversion of branch instructions

Improvement call-stack

BLR X1

Branch with link to register

Type	Branch direction	target	Source regs.	Dest. regs.	Written vals.
Unc. ind.	Taken	Taken_address	X1	X30	Return_addr

CVP-1 trace format

is branch?	Branch direction	Source regs.	Dest. regs.

ChampSim trace format

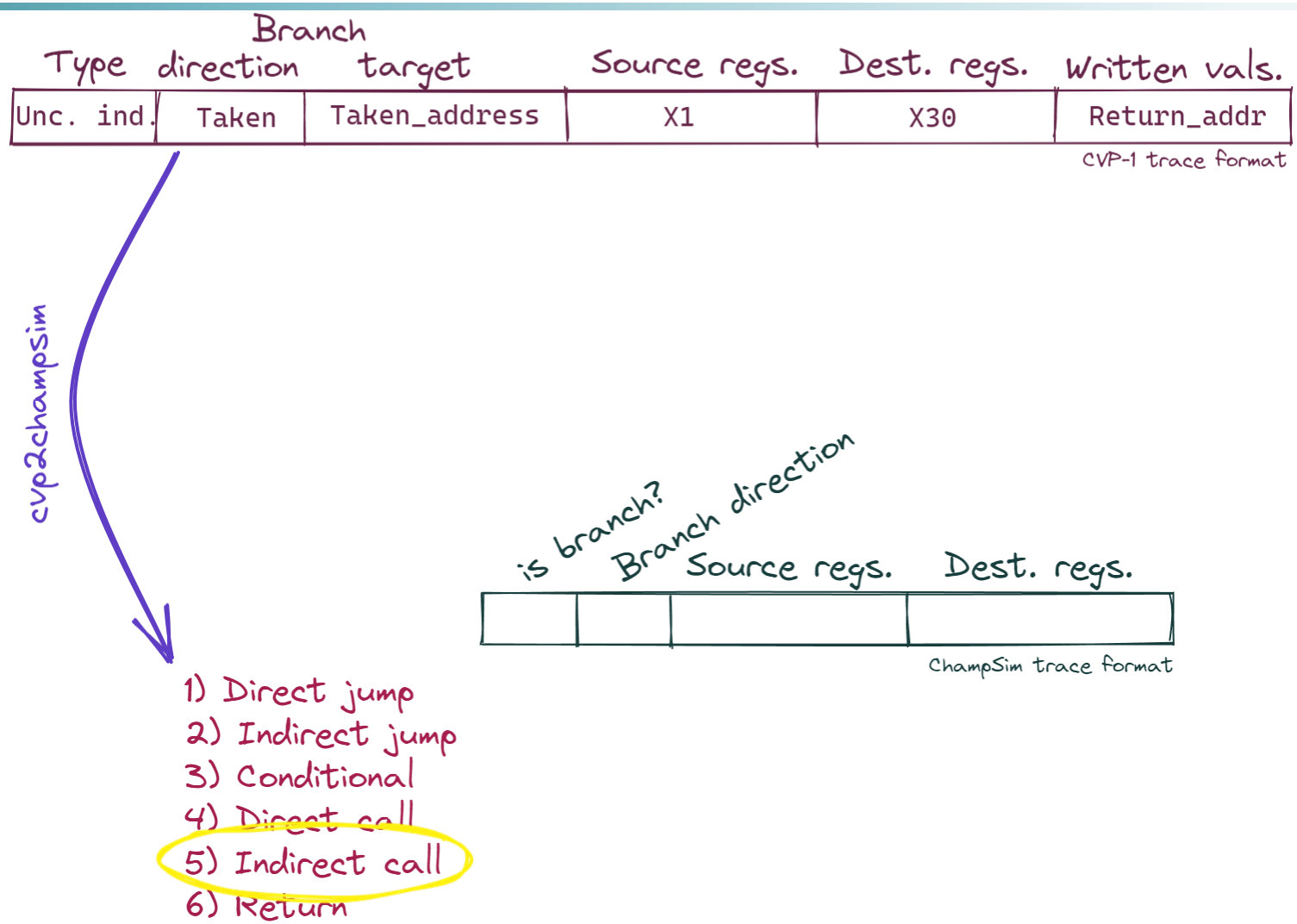
1) Direct jump
2) Indirect jump
3) Conditional
4) Direct call
5) Indirect call
6) Return

Conversion of branch instructions

Improvement call-stack

BLR X1

Branch with link to register



Conversion of branch instructions

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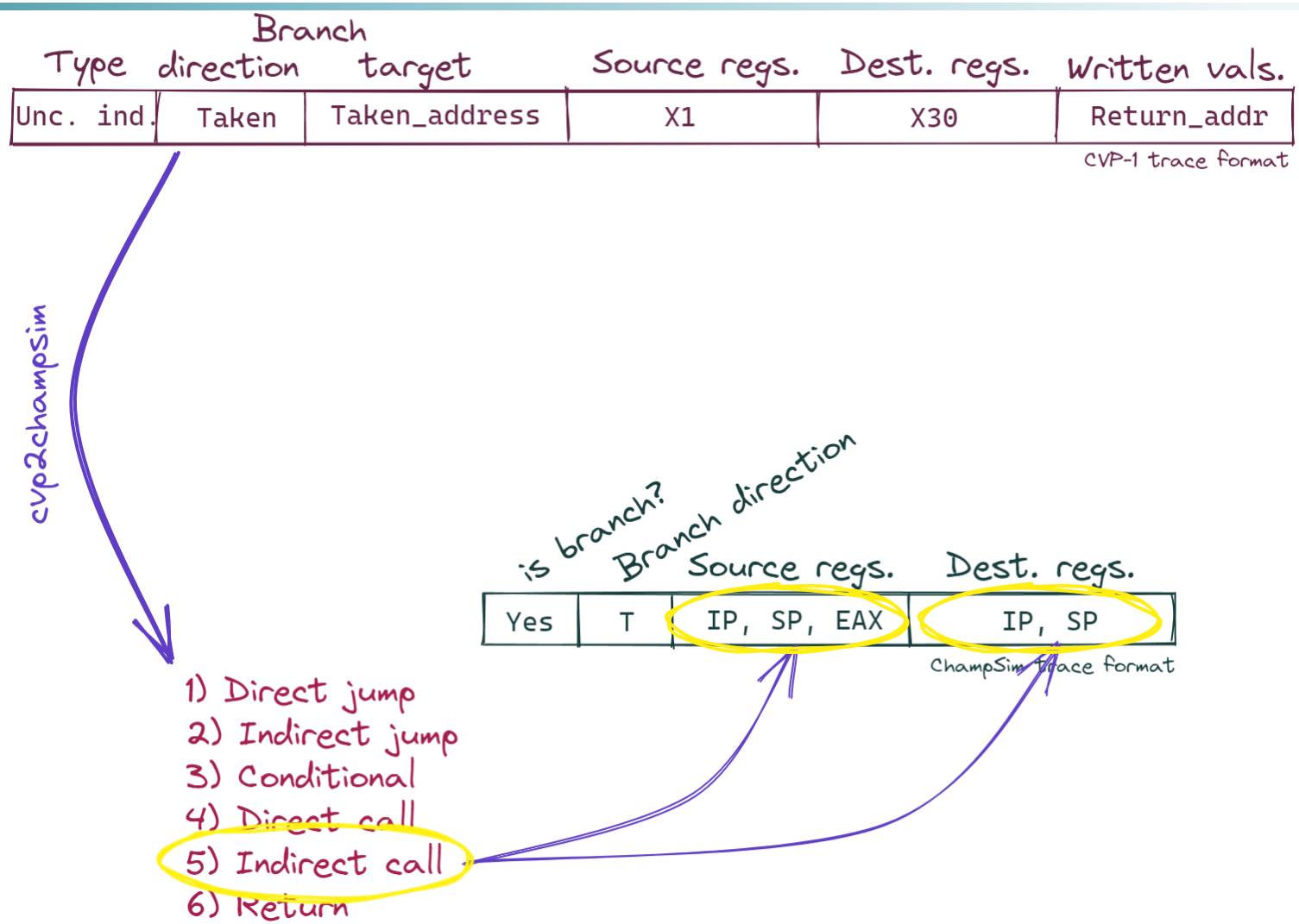

Conversion of branch instructions

Improvement call-stack

BLR X30

Branch with link to register

Type	Branch direction	target	Source regs.	Dest. regs.	Written vals.
Unc. ind.	Taken	Taken_address	X30	X30	Return_addr

CVP-1 trace format

is branch?	Branch direction	Source regs.	Dest. regs.

ChampSim trace format

Misclassifies BLR X30

1) Direct jump
2) Indirect jump
3) Conditional
4) Direct call
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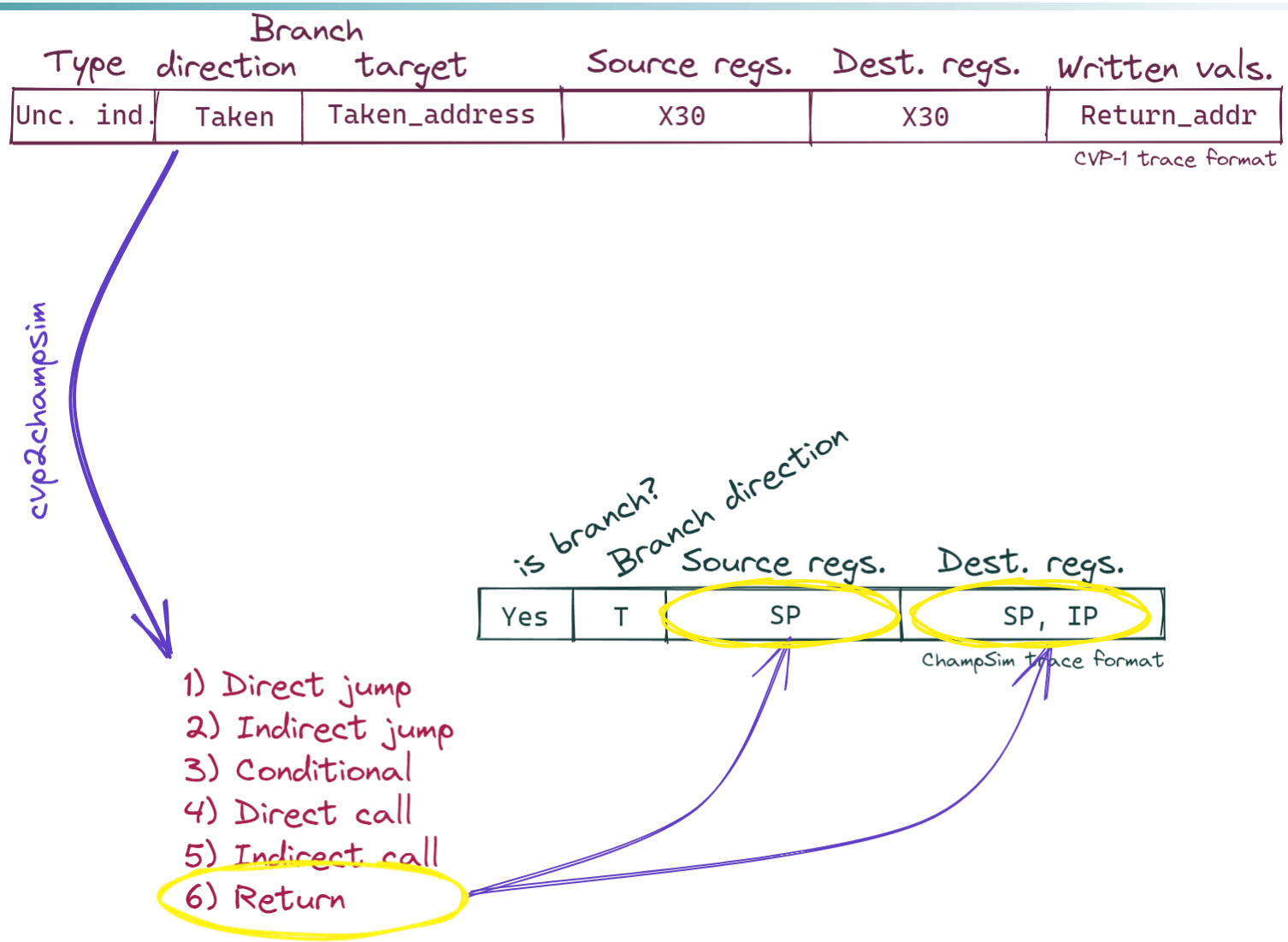
6) Return

Conversion of branch instructions

Improvement call-stack

BLR X30

Branch with link to register



Misclassifies BLR X30

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Type	Branch direction	Branch target	Source regs.	Dest. regs.	Written vals.
Unc. ind.	Taken	Taken_address	X30	X30	Return_addr

CVP-1 trace format

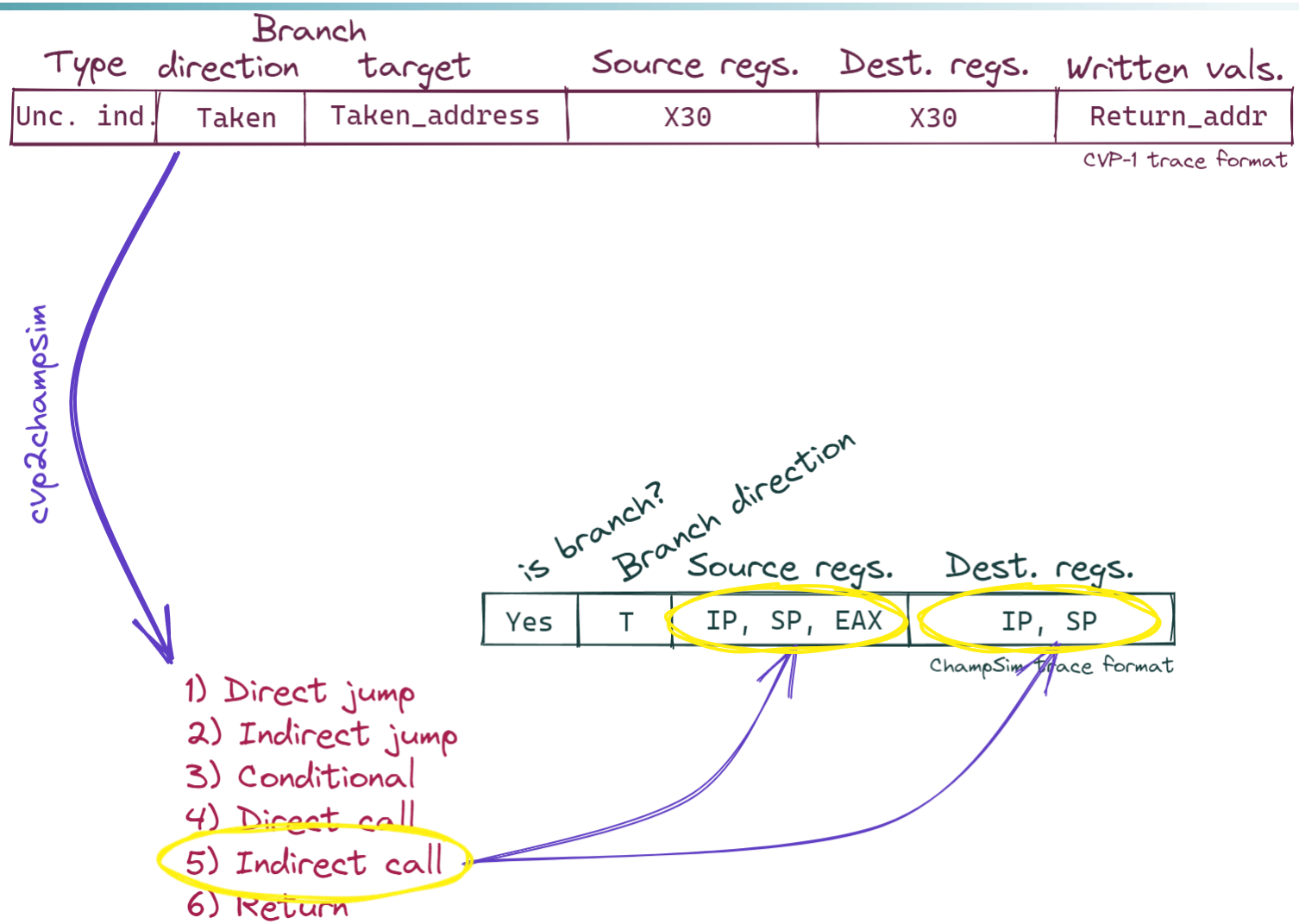
Fix the branch-type identification

Conversion of branch instructions

Improvement call-stack

BLR X30

Branch with link to register



Fix the branch-type identification

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  - Improvement flag-reg
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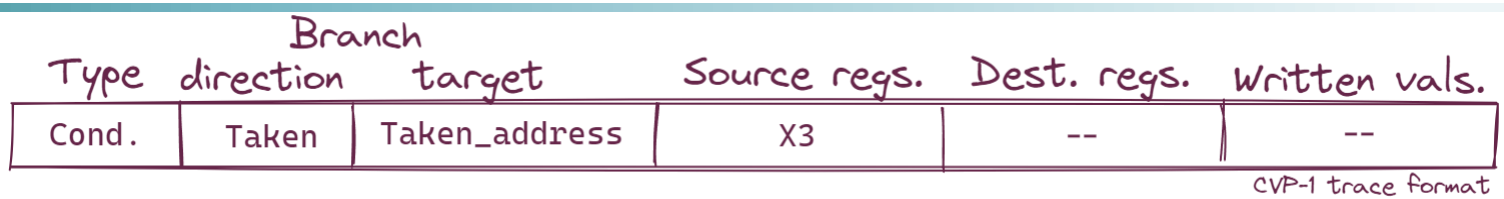
Conversion of branch instructions

Improvement branch-regs

```
CBZ X3, Taken_Address
```

Compare and branch on zero



Conversion of branch instructions

Improvement branch-regs

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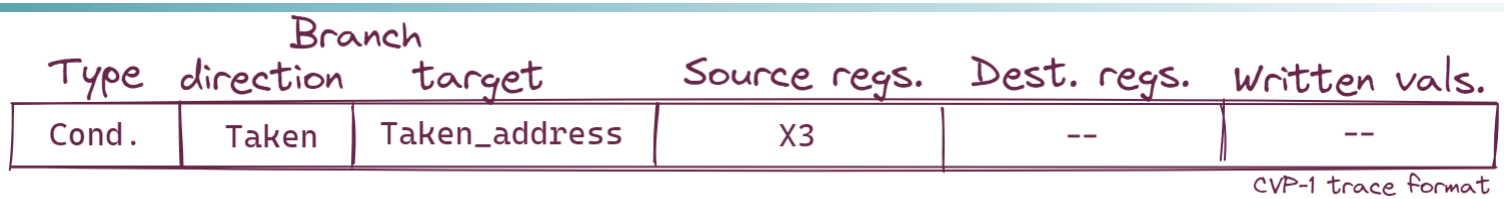

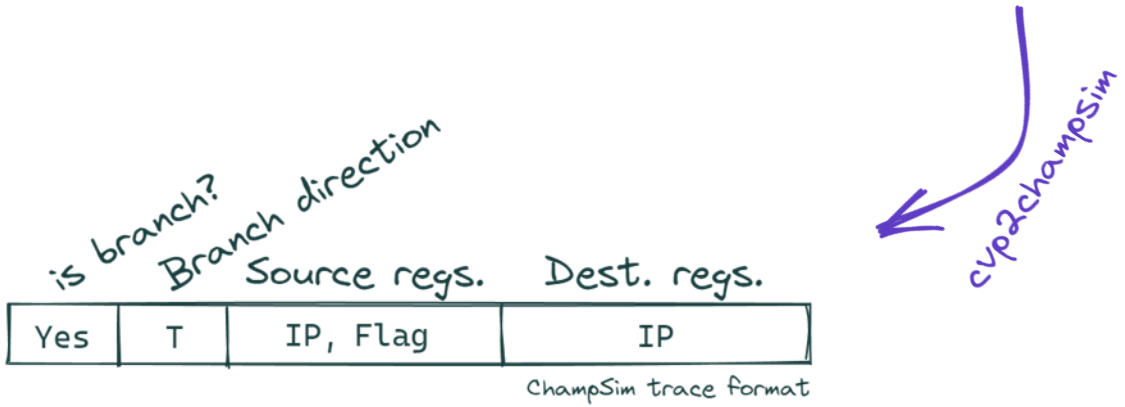

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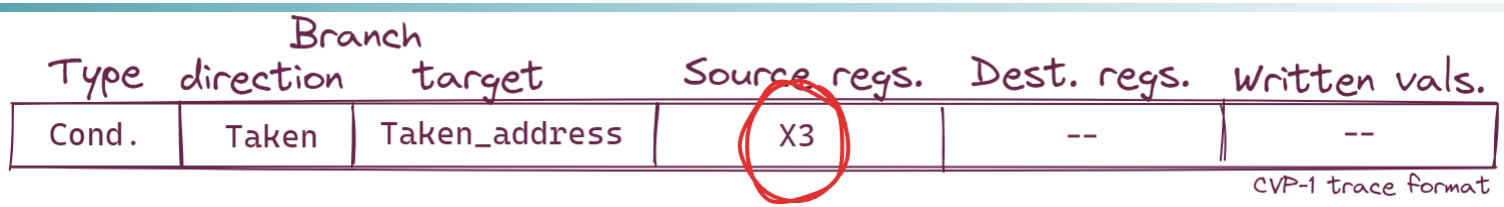

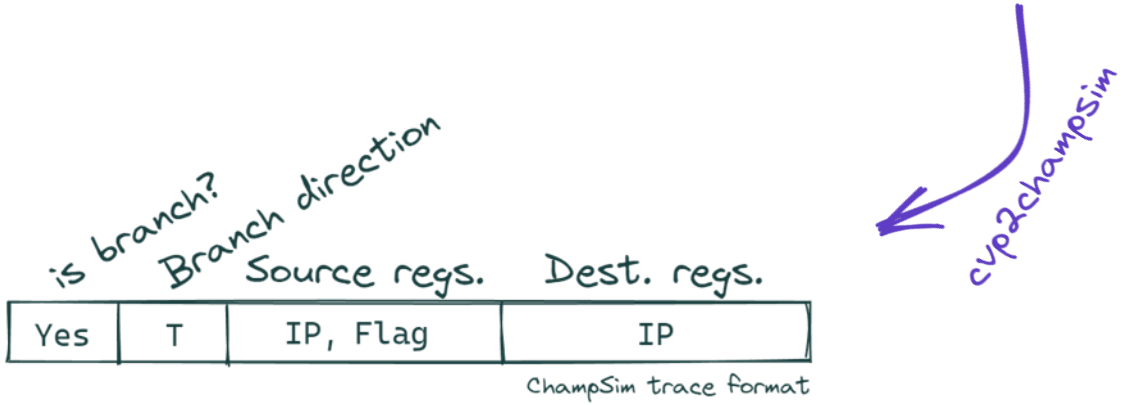

Registers of the CVP-1 branch instructions are not conveyed.

- Dependences with previous instructions are lost.

Conversion of branch instructions

Improvement branch-regs

```
CBZ X3, Taken_Address
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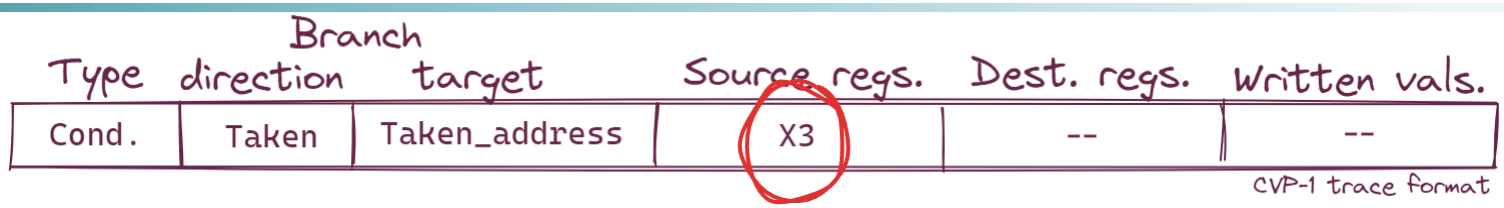
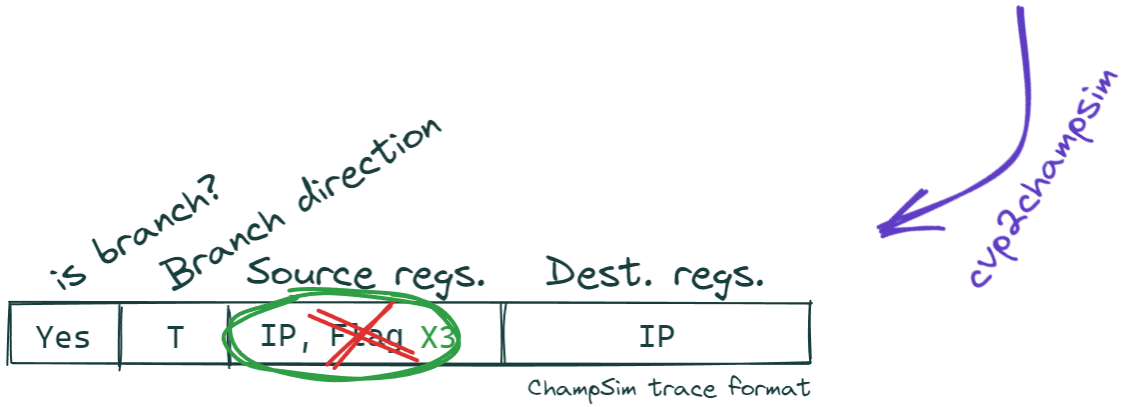
Compare and branch on zero



Convey the registers in the CVP-1 trace to preserve the original dependences.

- Applies similarly to the other types of branches.
- Minor change in ChampSim branch inference.



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Conversion of branch instructions

Improvement flag-reg

```
CMP X3, #0
```

Dependence through the flag register

```
BEQ Taken_Address
```

Branch if the Z flag is set

Conversion of branch instructions

Improvement flag-reg

```
CMP X3, #0
```

Type	Source regs.	Dest. regs.	Written vals.
Alu	X3	--	--

CVP-1 trace format

Dependence through the flag register

```
BEQ Taken_Address
```

Branch if the Z flag is set

Type	Branch direction	Branch target	Source regs.	Dest. regs.	Written vals.
Cond.	Taken	Taken_address	--	--	--

CVP-1 trace format

Special-purpose registers not present in the CVP trace.

Conversion of branch instructions

Improvement flag-reg

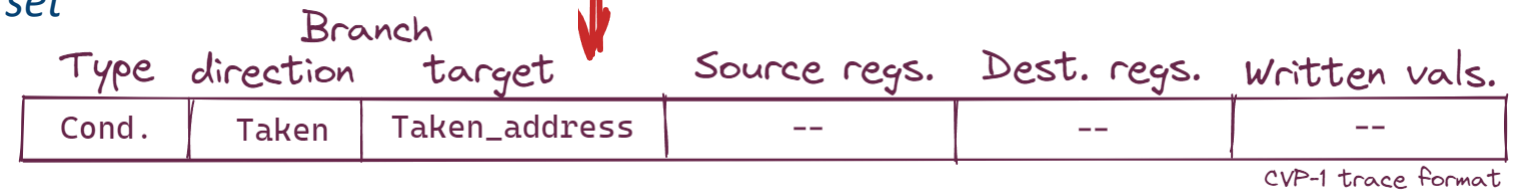
```
CMP X3, #0
```

Dependence through the flag register

Dependence lost

```
BEQ Taken_Address
```

Branch if the Z flag is set



Special-purpose registers not present in the CVP trace.

Conversion of branch instructions

Improvement flag-reg

```
CMP X3, #0
```

Type	Source regs.	Dest. regs.	Written vals.
Alu	X3	--	--

CVP-1 trace format

Dependence through the flag register

Dependence lost

```
BEQ Taken_Address
```

Branch if the Z flag is set

Type	Branch direction	Branch target	Source regs.	Dest. regs.	Written vals.
Cond.	Taken	Taken_address	--	--	--

CVP-1 trace format

cvp2champsim

is branch?	Branch direction	Source regs.	Dest. regs.
Yes	T	IP, Flag	IP

ChampSim trace format

Conversion of branch instructions

Improvement flag-reg

```
CMP X3, #0
```

Dependence through the flag register

```
BEQ Taken_Address
```

Branch if the Z flag is set

Dependence lost

Type	Source regs.	Dest. regs.	Written vals.
Alu	X3	--	--

CVP-1 trace format

cvp2champsim

is branch?	Branch direction	Source regs.	Dest. regs.
No	--	X3	Flag

ChampSim trace format

Type	Branch direction	Branch target	Source regs.	Dest. regs.	Written vals.
Cond.	Taken	Taken_address	--	--	--

CVP-1 trace format

cvp2champsim

is branch?	Branch direction	Source regs.	Dest. regs.
Yes	T	IP, Flag	IP

ChampSim trace format

Add the flag register as a destination to ALU and FP instructions without any.

Conversion of branch instructions

Improvement flag-reg

```
CMP X3, #0
```

Dependence through the flag register

```
BEQ Taken_Address
```

Branch if the Z flag is set

Type	Source regs.	Dest. regs.	Written vals.
Alu	X3	--	--

CVP-1 trace format

cvp2champsim

is branch?	Branch direction	Source regs.	Dest. regs.
No	--	X3	Flag

ChampSim trace format

Dependence lost

Type	Branch direction	Branch target	Source regs.	Dest. regs.	Written vals.
Cond.	Taken	Taken_address	--	--	--

CVP-1 trace format

cvp2champsim

is branch?	Branch direction	Source regs.	Dest. regs.
Yes	T	IP, Flag	IP

ChampSim trace format

Dependence restored

Add the flag register as a destination to ALU and FP instructions without any.

Outline

- Introduction
- Conversion of memory instructions
- Conversion of branch instructions
- Experimental evaluation
- Conclusion

Experimental evaluation
Setup

Analysis of the impact of the converter improvements.

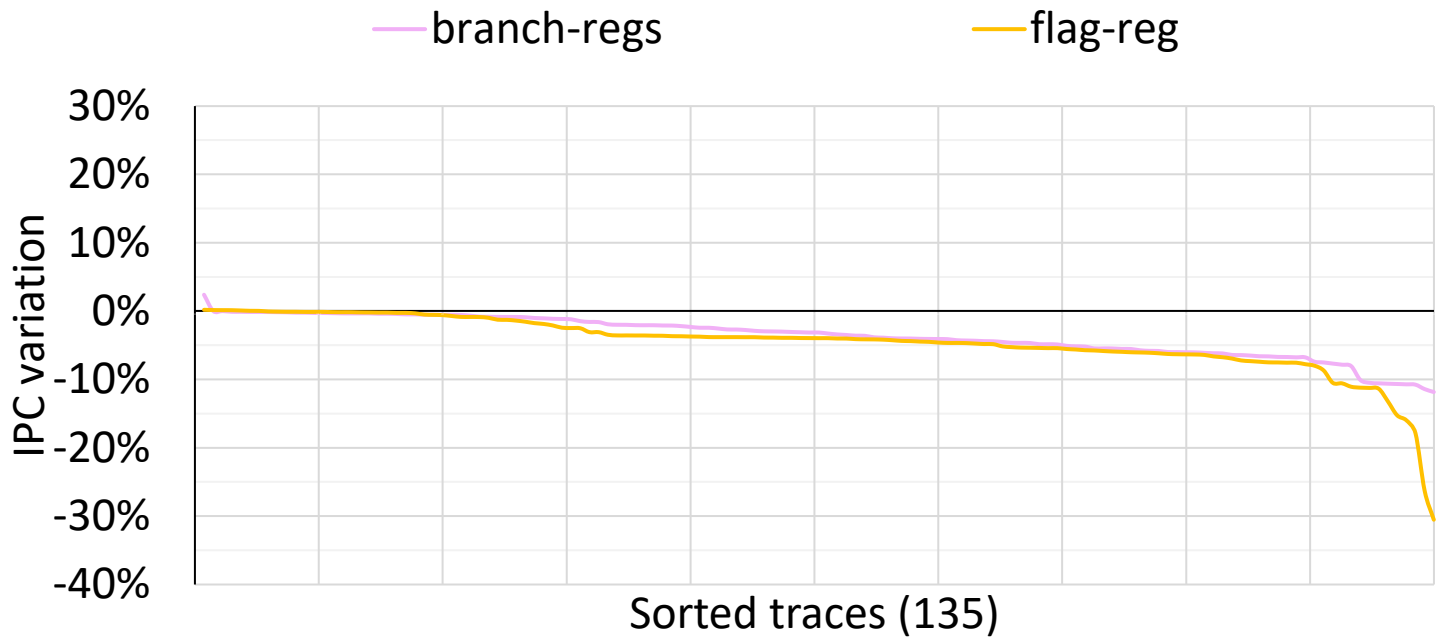
- CVP-1 public traces.
- ChampSim main branch (*commit 2bba2bd*).
- Processor configuration resembling Intel Icelake
  - 16K-entry BTB, 64KB ITTAGE, and TAGE-SC-L predictors.
  - Ip-stride prefetcher at the L1D cache and a next-line prefetcher at the L2 cache.

Reevaluation of the IPC-1 Championship (just for fun, prefetchers were tuned for the old traces).

- IPC-1 traces.
- ChampSim version provided in the championship.
- Original code of the prefetchers.

Experimental evaluation

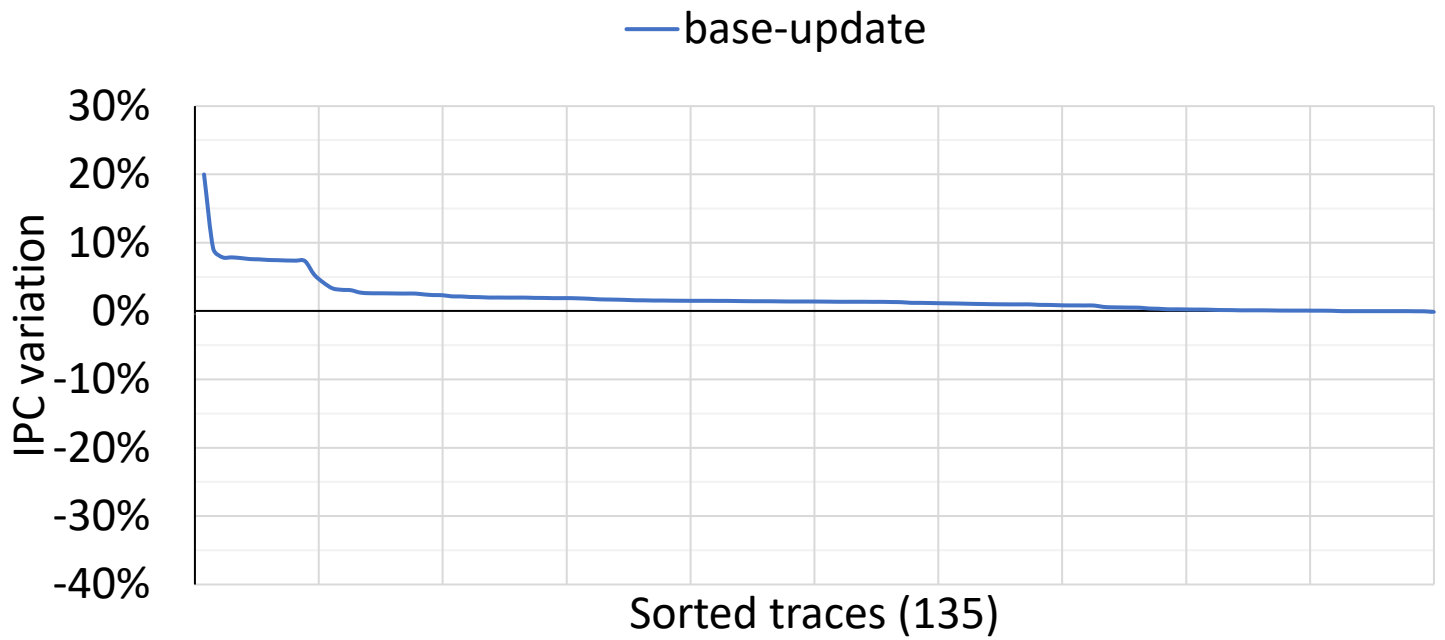
Performance impact



Improvements *flag-reg* and *branch-regs*:

- Restore the dependence of branches with previous instructions → Reduce IPC.

Experimental evaluation
Performance impact



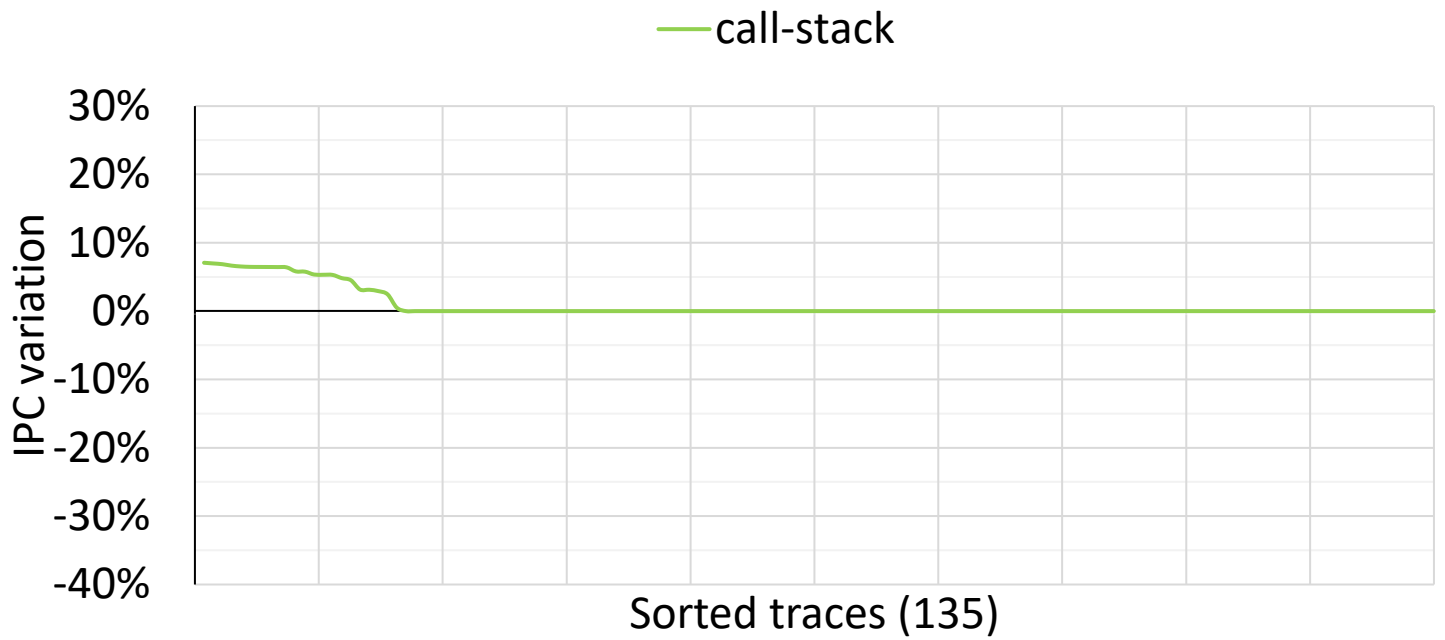
Improvements *flag-reg* and *branch-regs*:

- Restore the dependence of branches with previous instructions → Reduce IPC.

Improvement *base-update*:

- Makes base registers available earlier → Increase IPC.

Experimental evaluation
Performance impact



Improvements *flag-reg* and *branch-regs*:

- Restore the dependence of branches with previous instructions → Reduce IPC.

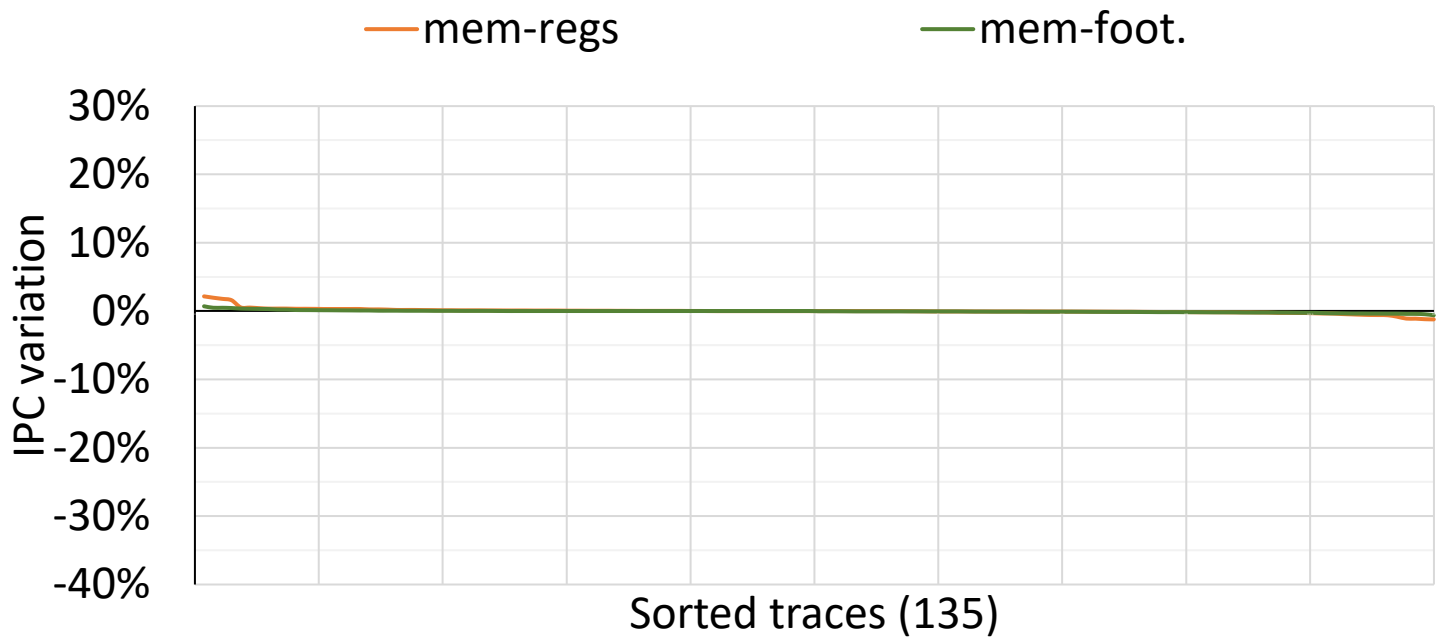
Improvement *base-update*:

- Makes base registers available earlier → Increase IPC.

Improvement *call-stack*:

- Reduces branch MPKI → Increase IPC.

Experimental evaluation
Performance impact

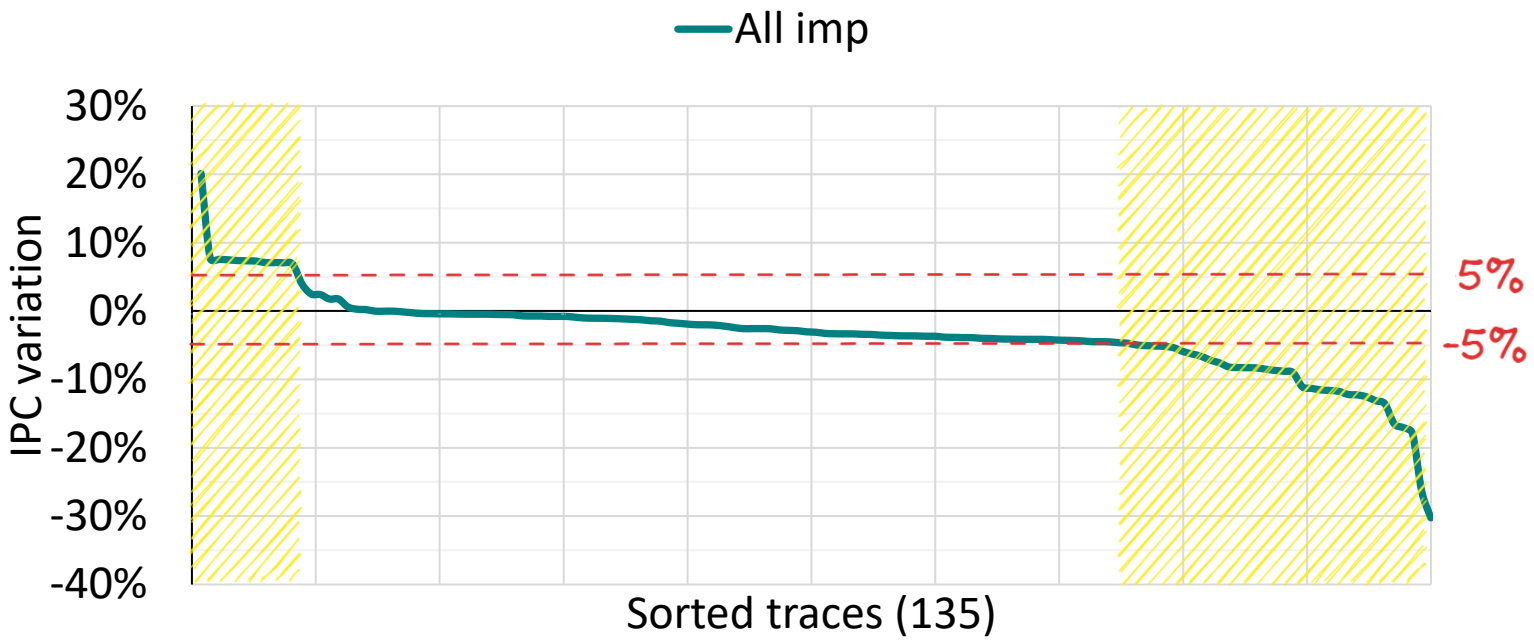


Improvements *mem-footprint* and *mem-regs* have a minimal impact:

- *Mem-footprint*: cacheblocks are accessed anyway plus are easy to prefetch.
- *Mem-regs*: no clear positive or negative effect but enables the base-update improvement.

Experimental evaluation

Performance impact



Performance deviates > 5% for 43 out of the 135 traces.

On average IPC reduces by 3.5%.

Experimental evaluation

Performance impact

Competition traces			Improved traces		
Rank	Prefetcher	SpeedUp	Rank	Prefetcher	SpeedUp
1	EPI	1.2951	1	EPI	1.3818
2	D-JOLT	1.2884	2	D-JOLT	1.3696
3	FNL+MMA	1.2861	3	JIP	1.3588
4	BARÇA	1.2832	4	BARÇA	1.3570
5	PIPS	1.2799	5	FNL+MMA	1.3517
6	JIP	1.2768	6	PIPS	1.3444
7	MANA	1.2658	7	MANA	1.3092
8	TAP	1.2351	8	TAP	1.2915

With the new traces, speedup grows for all prefetchers.

No big changes in the competition (except for JIP).

Conclusion

Our study highlights the need for carefully vetting the tools to conduct research.

We advocate for sharing tools, but

- Some are built with very specific uses in mind.
- Using them for a different purpose can lead to significant inaccuracies.

We should model the behavior of workloads as faithfully as possible.

We propose several improvements to the CVP-1 to Champsim trace converter:

- Better conveys the characteristics of the original workloads.
  - Performance difference greater than 5% in 1/3 of the traces.
- Easily adaptable to a new trace format.

Rebasing Microarchitectural Research with Industry Traces

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Thank you! Questions??

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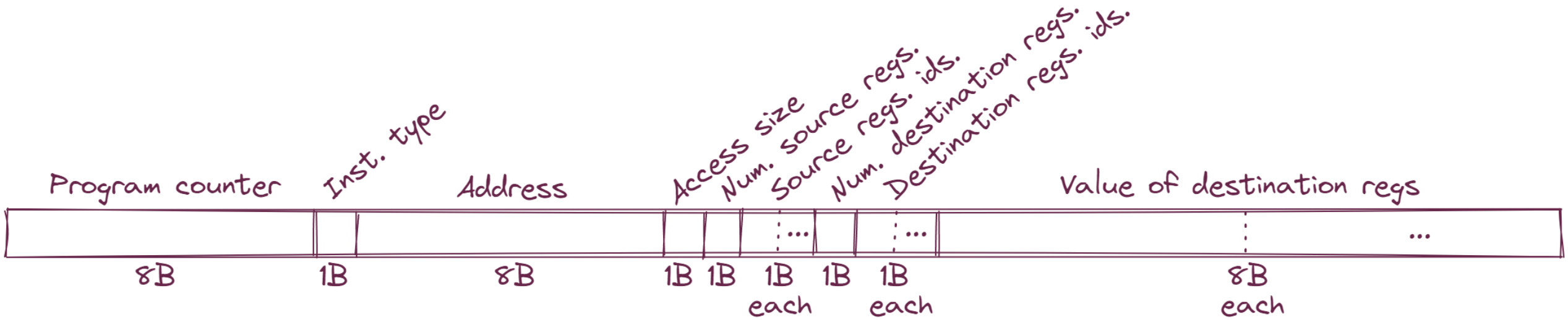
Conversion of memory instructions

Improvement mem-regs



CVP-1 trace format for memory instructions

Conversion of memory instructions

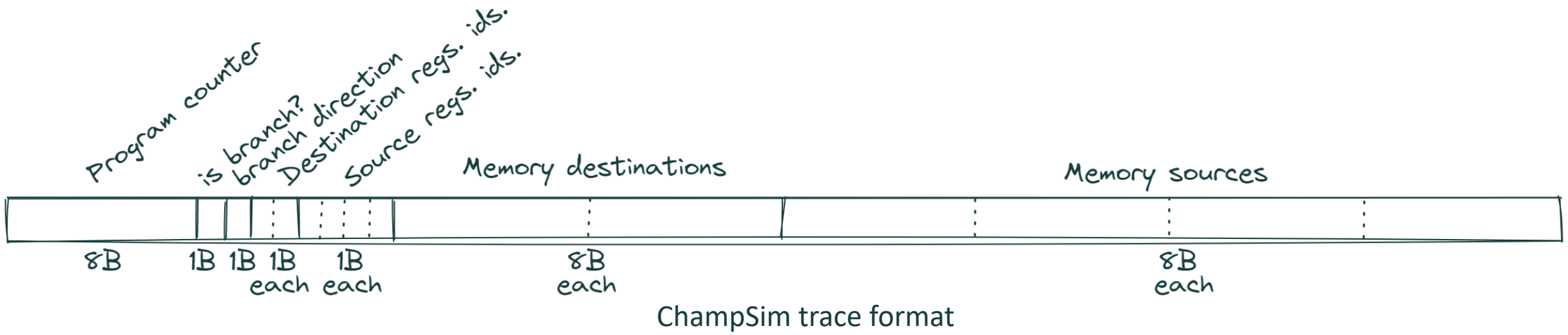
Improvement mem-regs

```
LDP X1, X0, [X0]
```

Load pair → X1 = Mem[X0], X0 = Mem[X0+8]

Type	Address	Size	Source regs.	Dest. regs.	Written vals.
load	addr	8	X0	X1, X0	Val1, Val0

CVP-1 trace format



ChampSim trace format